CEMTool Tutorial

Transistor circuits

Overview

This tutorial is part of the CEMWARE series. Each tutorial in this series will teach you a specific topic of common applications by explaining theoretical concepts and providing practical examples.

This tutorial is to demonstrate the use of CEMTool for solving electronics problems. In this tutorial, CEMTool will be used to solve problems involving metal-oxide semiconductor field effect and bipolar junction transistors. The general topics to be discussed in this chapter are dc model of BJT and MOSFET, biasing of discrete and integrated circuits, and frequency response of amplifiers.

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1. Bipolar junction transistors

Bipolar junction transistor (BJT) consists of two pn junctions connected back-to-back. The operation of the BJT depends on the flow of both majority and minority carriers. There are two types of BJT: npn and pnp transistors. The electronic symbols of the two types of transistors are shown in Figure 1.

The dc behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are

$$I_F = I_{ES}\left[\exp\left(\frac{V_{BE}}{V_T}\right)-1\right] \tag{1}$$

$$I_R = I_{CS}\left(\exp\left(\frac{V_{BC}}{V_T}\right)-1\right) \tag{2}$$

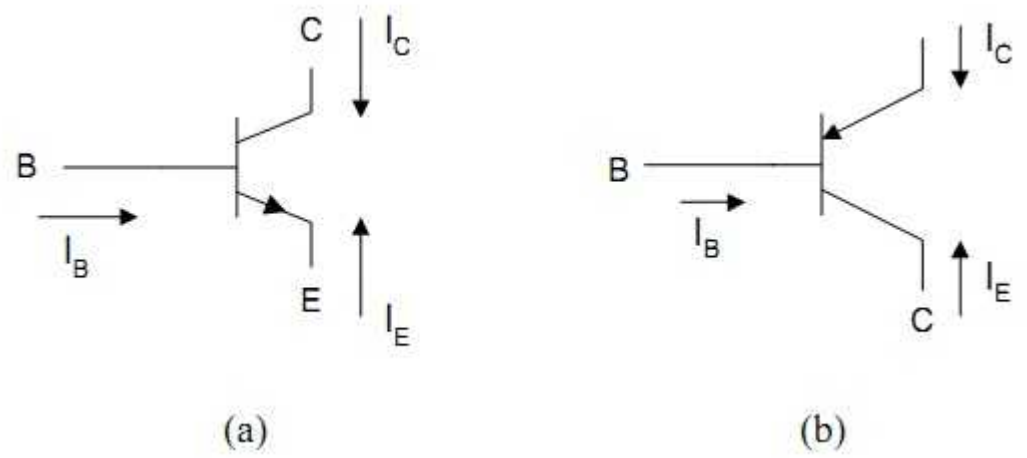

Figure 1: (a) NPN transistor (b) PNP transistor

and $I_C = \alpha_F I_F - I_R$ (3)

$I_E = -I_F + \alpha_R I_R$ (4)

and $I_B = (1-\alpha_F) I_F + (1-\alpha_R) I_R$ (5)

where I_{ES} *and* I_{CS} are the base-emitter and base-collector saturation currents, respectively

α_R is large signal reverse current gain of a common-base configuration

α_F is large signal forward current gain of the common-base configuration.

and $V_T = \frac{kT}{q}$ (6)

where k is the Boltzmann's constant (k = 1.381x10^{-23}V.C/^{o}K),

T is the absolute temperature in degrees Kelvin, and

q is the charge of an electron (q = 1.602x 10^{-19} C).

The forward and reverse current gains are related by the expression $\alpha_R I_{CS} = \alpha_F I_{ES} = I_S$ (7)

where I_S is the BJT transport saturation current.

The parameters α_R and α_F are influenced by impurity concentrations and junction depths. The saturation current, I_S, can be expressed as $I_S = J_S A$ (8)

where A is the area of the emitter and

J_S is the transport saturation current density, and it can be further expressed as

$$J_S = \frac{qD_n n_i^2}{Q_B} \quad (9)$$

where D_n is the average effective electron diffusion constant

n_i is the intrinsic carrier concentration in silicon (n_i = 1.45x10^{10}atoms/cm^3 at 300^{o}K)

QB is the number of doping atoms in the base per unit area.

Example 1

Assume that a BJT has an emitter area of 5.0 mil^2, β_F =120, β_R = 0.3 transport current density, J_S =2*10^{-10} μA/mil^2 and T = 300°K. Plot I_E versus V_{BE} for V_{BC} = -1V. Assume 0 < V_{BE} < 0.7 V.

Solution

From Equations 1, 2, 3 and 4 we can write the following CEMTool program.

```
%Input characteristics of a BJT
k=1.381e-23; temp=300; q=1.602e-19;
cur_den=2e-10; area=5.0; beta_f=120; beta_r=0.3
vt=k*temp/q; is=cur_den*area;
alpha_f=beta_f/(1+beta_f);
alpha_r = beta_r/(1+beta_r);
ies=is/alpha_f;
vbe=0.3:0.65:0.01;
ics=is/alpha_r;
m=length(vbe)
for (i = 1;i<=m ;i++)
{ ifr(i) = ies*exp((vbe(i)/vt)-1);
  ir1(i) = ics*exp((-1.0/vt)-1);
  ie1(i) = abs(-ifr(i) + alpha_r*ir1(i));
}
plot(vbe,ie1)
title("Input characteristics")
xlabel("Base-emitter voltage, V")
ylabel("Emitter current, A")
```

Figure 2 shows the input characteristics.

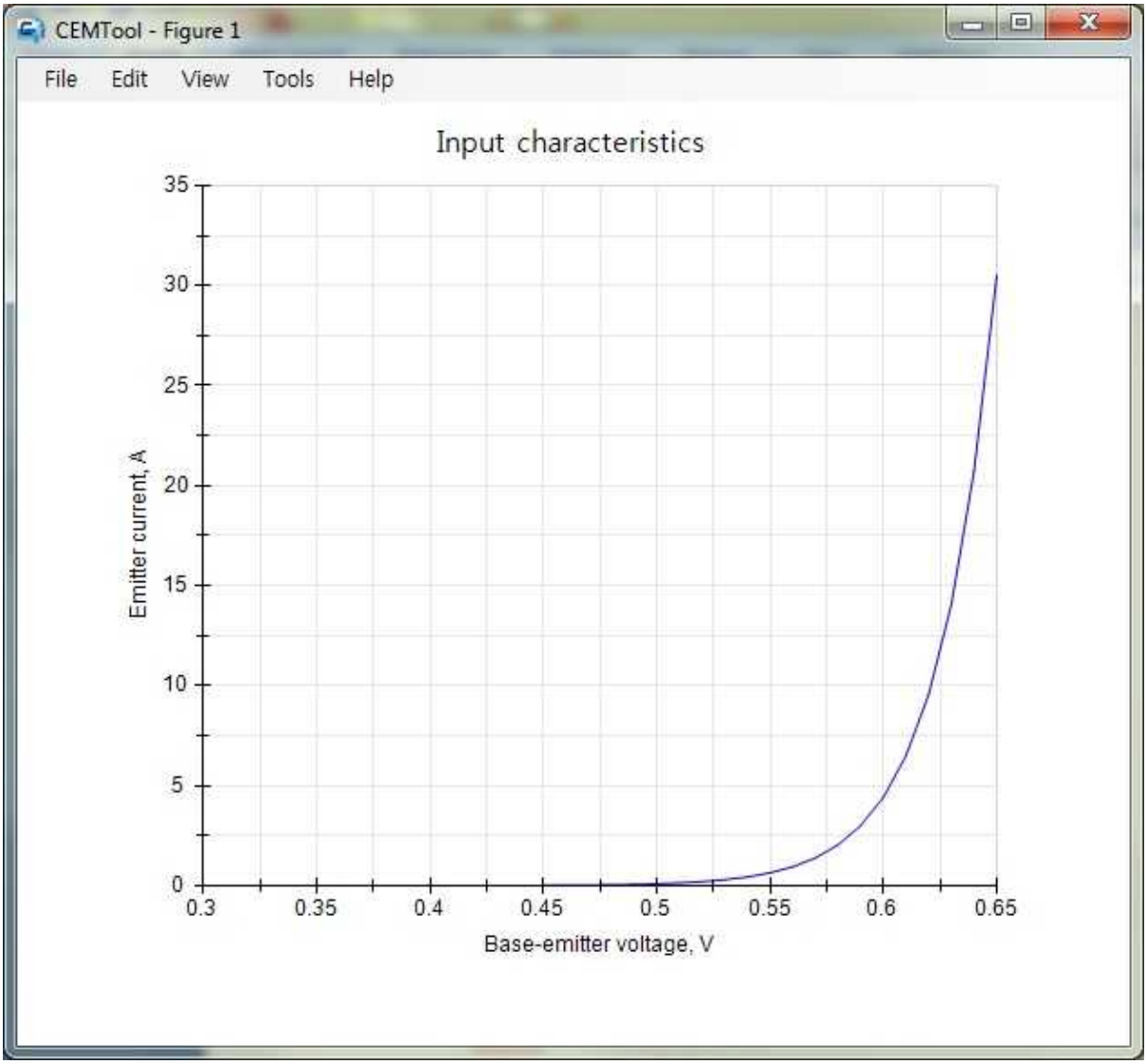

Figure 2: Input characteristics of a bipolar junction transistor

2. Biasing BJT discrete circuits

2.1 Self-bias circuit

One of the most frequently used biasing circuits for discrete transistor circuits is the self-bias of the emitter-bias circuit shown in Figure 3. The emitter resistance, R_E, provides stabilization of the bias point. V_{BB} and R_B are the Thevenin equivalent parameters for the base bias circuit. Using Kirchoff's Voltage Law for the base circuit, we have

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E \tag{10}$$

Applying KVL at the output loop of Figure 3b gives $V_{CE} = V_{CC} = I_C R_C - I_E R_E$ (11)

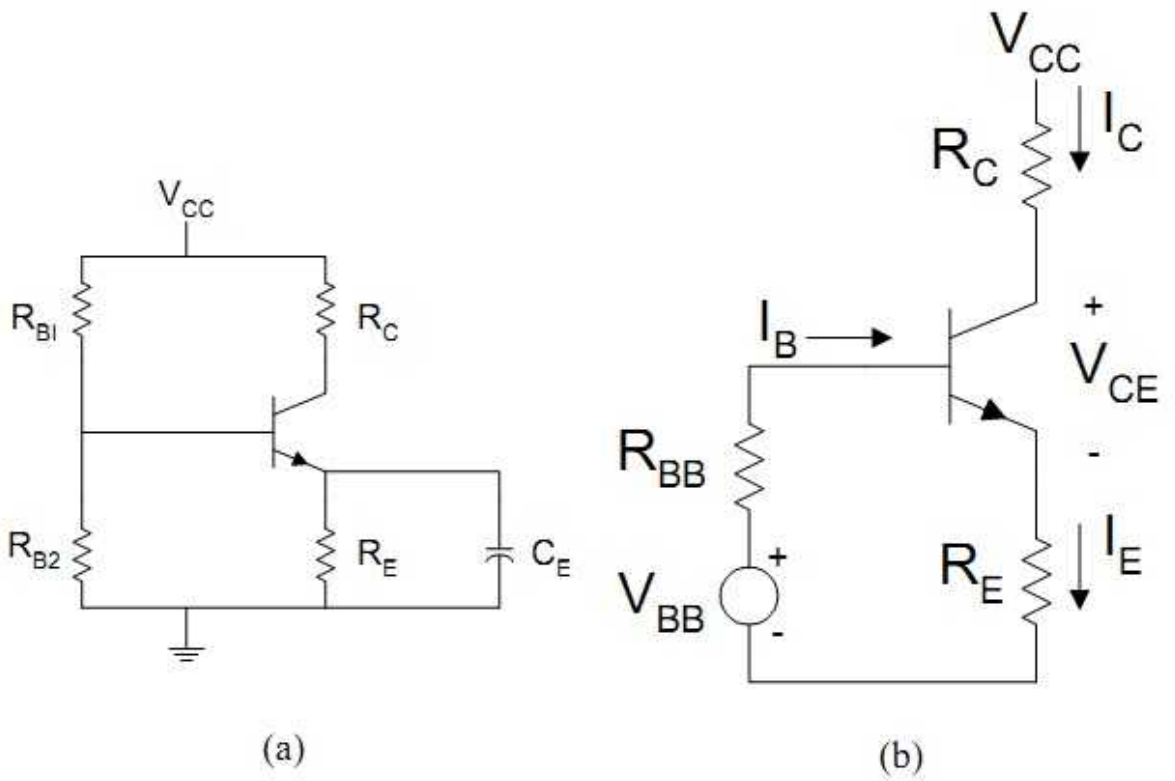

Figure 3: (a) Self-bias circuit (b) DC equivalent circuit of (a)

2.2 Bias stability

Equation 11 gives the parameters that influence the bias current I_C. The voltage V_{BB} depends on the supply voltage V_{CC}. In some cases, V_{CC} would vary with I_C, but by using a stabilized voltage supply we can ignore the changes in V_{CC}, and hence V_{BB}. The changes in the resistances R_{BB} and R_E are negligible. There is a variation of β_F with respect to changes in I_C. A typical plot of β_F versus I_C is shown in Figure 4.

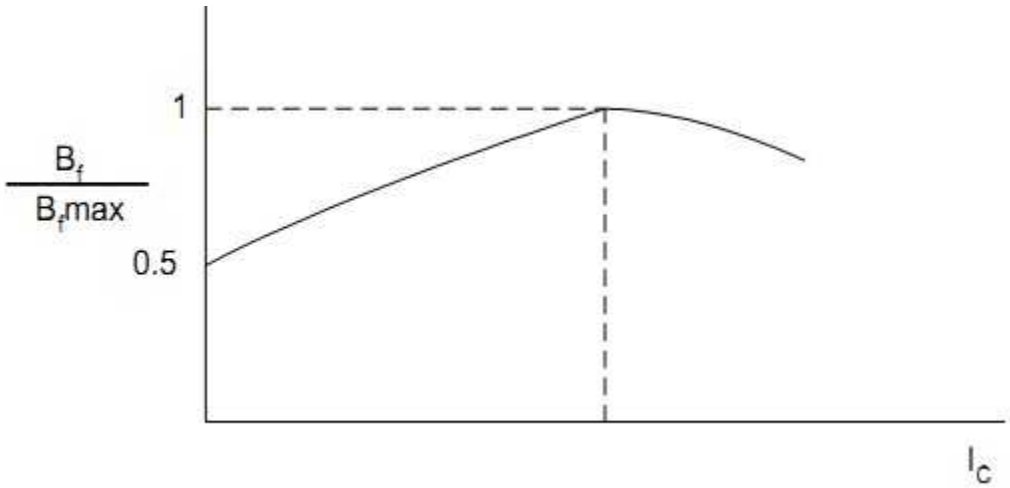

Figure 4: Normalized plot of β_F as a function of collector current

Temperature changes cause two transistor parameters to change. These are (1) base-emitter voltage (V_{BE}) and (2) collector leakage current between the base and collector (I_{CBO}). The variation on V_{BE} with temperature is similar to the changes of the pn junction diode voltage with temperature. For silicon transistors, the voltage V_{BE} varies almost linearly with temperature as

$$\Delta V_{BE} \approx -2\left(T_2 - T_1\right) \quad mV \tag{12}$$

where T1 and T2 are in degrees Celsius.

The collector-to-base leakage current, I_{CBO}, approximately doubles every 10° temperature rise. If I_{CBO1} is the reverse leakage current at room temperature (25°C), then $I_{CBO2} = 2^{\left(T_2 - \frac{25^o C}{10}\right)} I_{CBO1}$

and $\Delta I_{CBO} = I_{CBO2} - I_{CBO1} = I = I_{CBO}\left[2^{\left(T_2 - \frac{25^o C}{10}\right)} - 1\right]$ (13)

For small parameter changes, a change in collector current is given as

$$\Delta I_C = S_V \Delta V_{BE} + S_\beta \Delta \beta_F + S_I \Delta I_{CBO} + S_{VCC} \Delta V_{CC} \tag{14}$$

where S is the stability factors.

And $S_V = \frac{dI_C}{dV_{BE}} = -\frac{1}{\frac{R_B}{\beta_F} + R_E\left(\beta_F + \frac{1}{\beta_F}\right)}$ (15)

$$S_{VCC} = \frac{V_{CC} - V_{CE}}{R_C + \frac{R_E}{\alpha_F}} \tag{16}$$

$$S_I = \frac{\partial I_C}{\partial I_{CBO}} = \frac{R_{BB} + R_E}{\frac{\left(R_{BB} + R_E\right)}{\beta_F} + R_E} \tag{17}$$

$$S_\beta = \frac{\partial I_C}{\partial \beta} = \frac{\left(R_B + R_E\right)\left[V_{BB} - V_{BE} + \left(R_B + R_E\right) I_{CBO}\right]}{\left(R_B + R_E + \beta R_E\right)^2} \tag{18}$$

The following example shows the use of CEMTool for finding the changes in the quiescent point of a transistor due variations in temperature, base-to-emitter voltage and common emitter current gain.

Example 3:

The self-bias circuit of Figure 3 has the following element values: $R_{B1} = 50K, R_{B2} = 10K,$ $R_E = 1.2K, R_C = 6.8K,$ β_F varies from 150 to 200 and V_{CC} is 10±0.05V. I_{CBO} is 1 μA at 25°C. Calculate the collector current at 25°C and plot the change in collector current for temperatures between 25 and 100°C. Assume V_{BE} and β_F at 25°C are 0.7V and 150, respectively.

Solution

Equations 10, and 11 can be used to calculate the collector current. At each temperature, the stability factors are calculated using Equations 15, 16, 17 and 18. The changes in V_{BE} and I_{CBO} with temperature are obtained using Equations 12 and 13, respectively. The change in I_C for each temperature is calculated using Equation 14.

CEMTool script

```
% Bias stability
%
rb1=50e3; rb2=10e3; re=1.2e3; rc=6.8e3;
vcc=10; vbe=0.7; icbo25=1e-6; beta=(150+200)/2;
vbb=vcc*rb2/(rb1+rb2);
rb=rb1*rb2/(rb1+rb2);
ic=beta*(vbb-vbe)/(rb+(beta+1)*re);

%stability factors are calculated
svbe=-beta/(rb+(beta+1)*re);
alpha=beta/(beta+1);
svcc=1/(rc + (re/alpha));
svicbo=(rb+re)/(re+(rb+re)/alpha);
sbeta=((rb+re)*(vbb-vbe+icbo25*(rb+re))/(rb+re+beta*re)^2);
% Calculate changes in Ic for various temperatures

t=25:100:1;
len_t = length(t);
dbeta = 50; dvcc=0.1;
for (i=1;i<=len_t;i++)
{          dvbe(i)= -2e-3*(t(i)-25);
          dicbo(i)=icbo25*(2^((t(i)-25)/10)-1);
          dic(i)=svbe*dvbe(i)+svcc*dvcc...
   +svicbo+dicbo(i)+sbeta*dbeta;
}
plot(t,dicbo)
title("Change in collector current vs. temperature")
xlabel("Temperature, degree C")
ylabel("Change in collector current, A")
```

Figure 5 shows I_C versus temperature.

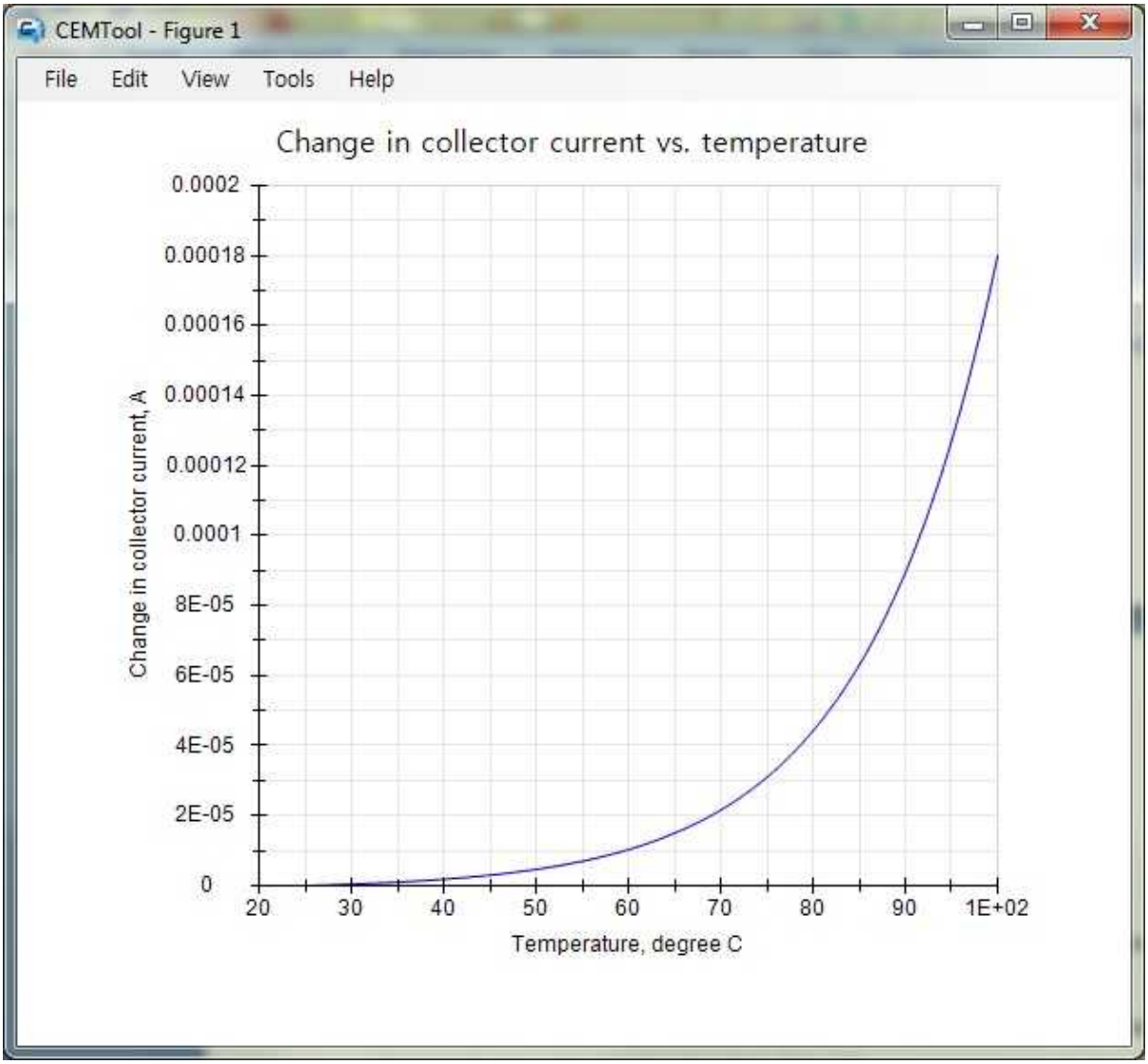

Figure 5: I_C versus temperature

3. Integrated circuit biasing

Biasing schemes for discrete electronic circuits are not suitable for integrated circuits (IC) because of the large number of resistors and the large coupling and bypass capacitor required for biasing discrete electronic circuits. It is uneconomical to fabricate IC resistors since they take a disproportionately large area on an IC chip. In addition, it is almost impossible to fabricate IC inductors. Biasing of ICs is done using mostly transistors that are connected to create constant current sources. Examples of integrated circuit biasing schemes are discussed in this section.

3.1 Simple current mirror

A simple current mirror is shown in Figure 6. The current mirror consists of two matched transistors Q_1 and Q_2 with their bases and emitters connected. The transistor Q_1 is connected as a diode by shorting the base to its collector.

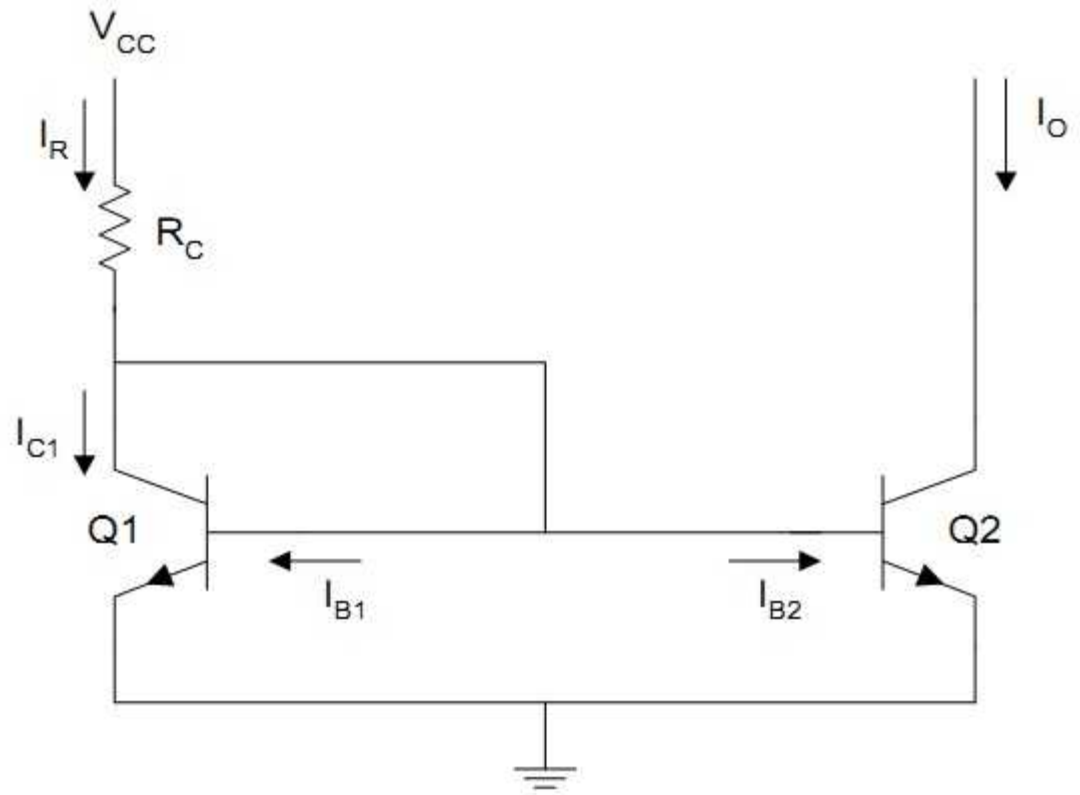

Figure 6: Simple current mirror

From figure 6, we observe that $I_R = \dfrac{V_{CC} - V_{BE}}{R_C}$ (19)

Thus, $I_R = I_{E1} + \dfrac{I_{E2}}{\beta+1} \approx I_{E2}\left[1 + \dfrac{1}{\beta+1}\right] = \left[\dfrac{\beta+2}{\beta+1}\right] I_{E2}$ (20)

3.2 Wilson current source

The Wilson current source, shown in Figure 7, achieves high output resistance and an output current that is less dependent on transistor β_F. To obtain an expression for the output current, we assume that all three transistors are identical. Thus

$$I_0 = \left(\frac{\beta_F^2 + 2\beta_F}{\beta_F^2 + 2\beta_F + 2}\right) I_R = \left(1 - \frac{2}{\beta_F^2 + 2\beta_F + 2}\right) I_R \quad (21)$$

So that, β has little effect on the output current, and $I_R = \dfrac{V_{CC} - V_{BE3} - V_{BE1}}{R_C}$ (22)

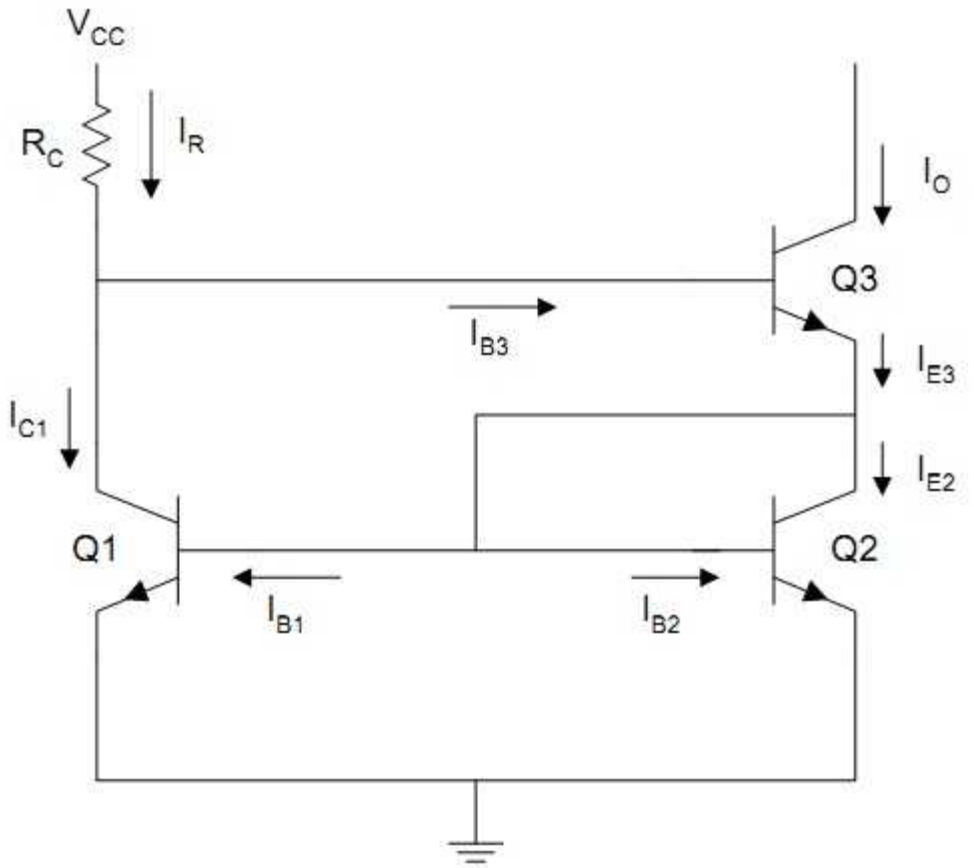

Figure 7: Wilson current source

Example 4:

For Figures 6 and 7, what are the percentage difference between the reference and output currents for the β_F from 40 to 200. Assume that for both figures, V_{VCC} =10, R_{KC} = 50 Ω and V_{VBE} = 0.7

Solution

We use Equation 19 to calculate IR and Equation 20 to find I_0 of the simple current mirror. Similarly, we use Equation 22 to find IR and Equation 21 to calculate I_0 of the Wilson current source.

CEMTool script

```
% Integrated circuit Biasing
vcc=10; rc=50e3; vbe=0.7;
beta =40:200:5;   ir1=(vcc-vbe)/rc;
ir2=(vcc-2*vbe)/rc;   m=length(beta);
for (i=1;i<=m;i++)
{    io1(i) = beta(i)*ir1/(beta(i) + 2);
    pd1(i)=abs((io1(i)-ir1)*100/ir1);
```

```
    io2(i)=(beta(i)^2+2*beta(i))/(beta(i)^2+2*beta(i)+2);
    pd2(i)=abs((io2(i)*ir2-ir2)*100/ir2);
}
subplot(2,1,1), plot(beta,pd1)
title("error for simple current mirror")
xlabel("Transistor beta")
ylabel("Percentage error")
subplot(2,1,2),plot(beta,pd2)
xlabel("Transistor beta")
ylabel("Percentage error")
title("Error for Wilson current source")
```

Figure 8 shows the percentage errors obtained for the simple current mirror and Wilson current source.

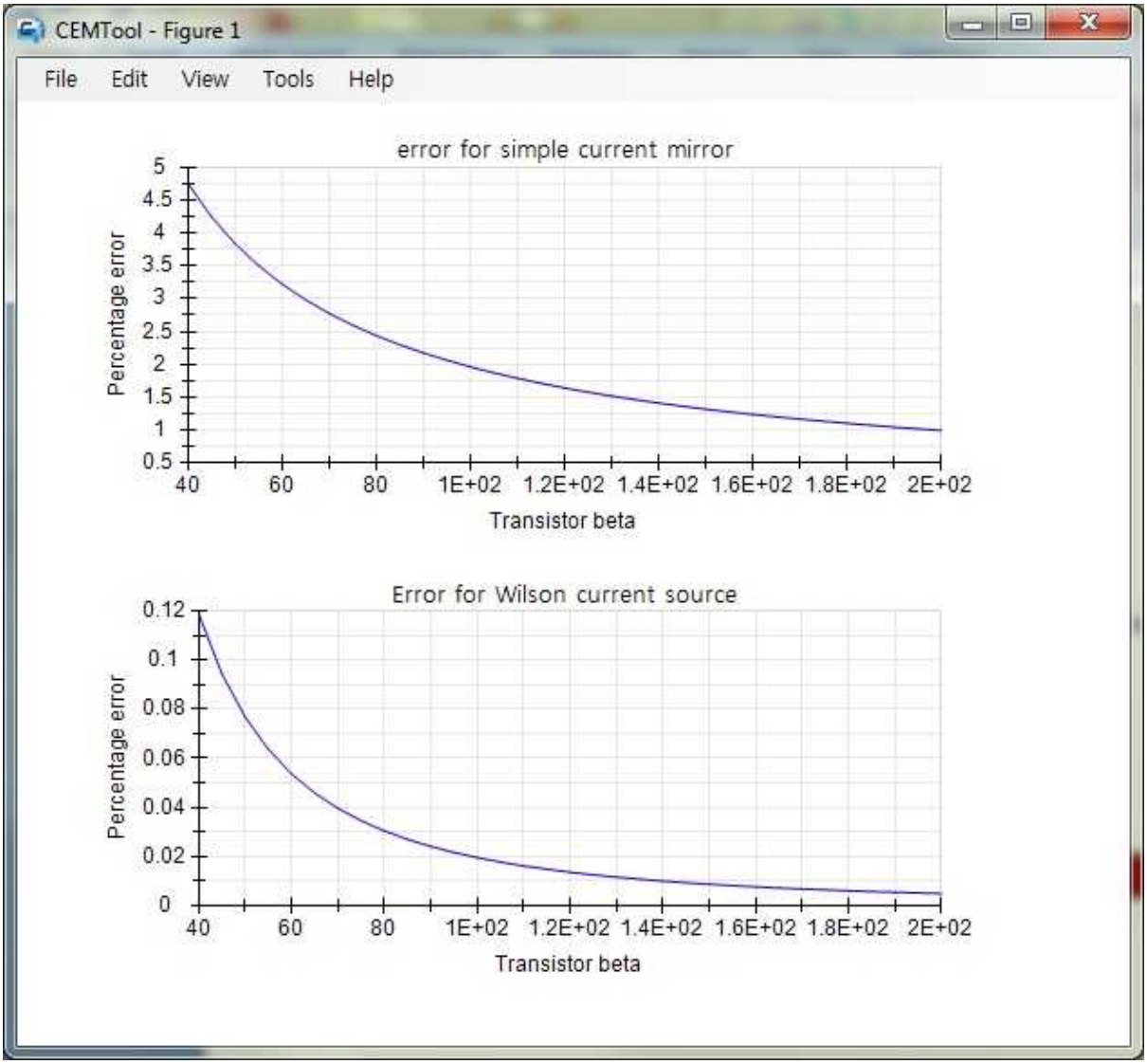

Figure 8: Percentage error between reference and output currents for simple current mirror and wilson current source

4. Frequency response of common emitter apmplifier

The common-emitter amplifier, shown in Figure 9, is capable of generating a relatively high current and voltage gains. The input resistance is medium and is essentially independent of the load resistance R_L. The output resistance is relatively high and is essentially independent of the source resistance.

The coupling capacitor, C_{C1}, couples the source voltage v_S to the biasing network. Coupling capacitor C_{C2} connects the collector resistance R_C to the load R_L. The bypass capacitance C_E is used to increase the midband gain, since it effectively short circuits the emitter resistance R_E at midband frequencies. The resistance R_E is needed for bias stability. The external capacitors C_{C1}, C_{C2} , C_E will influence the low frequency response of the common emitter amplifier. The internal capacitances of the transistor will influence the high frequency cut-off. The overall gain of the

common-emitter amplifier can be written as

$$A(s) = \frac{A_m s^2 (s + \omega_z)}{(s + \omega_{L1})(s + \omega_{L2})(s + \omega_{L3})(1 + s/\omega_H)} \tag{23}$$

where A_M is the midband gain.

ω_H is the frequency of the dominant high frequency pole

$\omega_{L1}, \omega_{L2}, \omega_{L3}$ are low frequency poles introduced by the coupling and bypass capacitors

ω_Z is the zero introduced by the bypass capacitor.

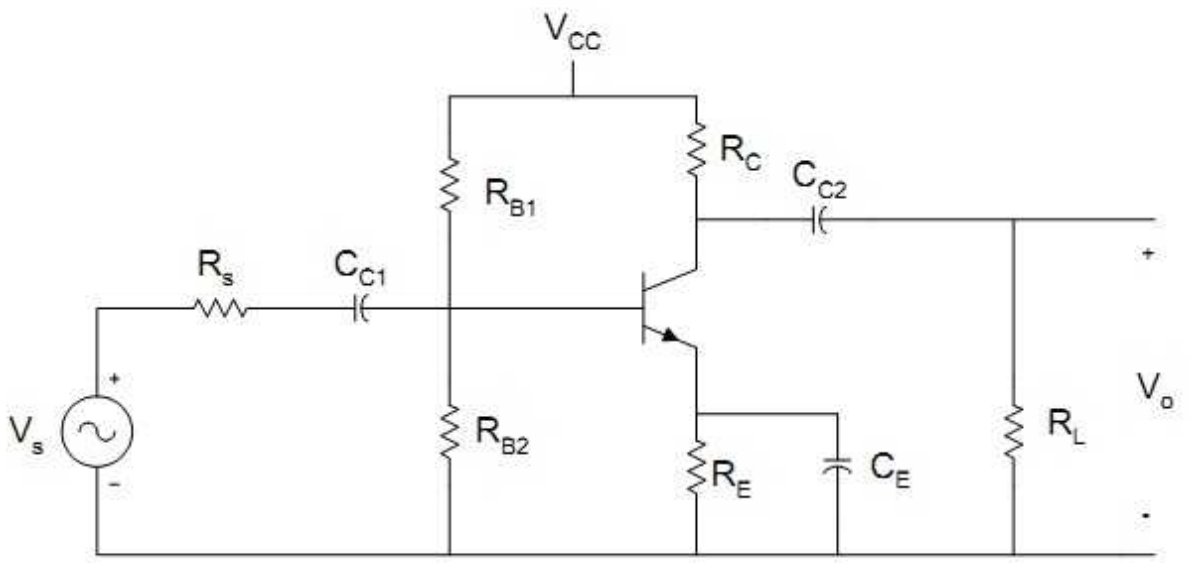

Figure 9: Common emitter amplifier

The midband gain is obtained by short circuiting all the external capacitors and open circuiting the internal capacitors. Figure 10 shows the equivalent for calculating the midband gain.

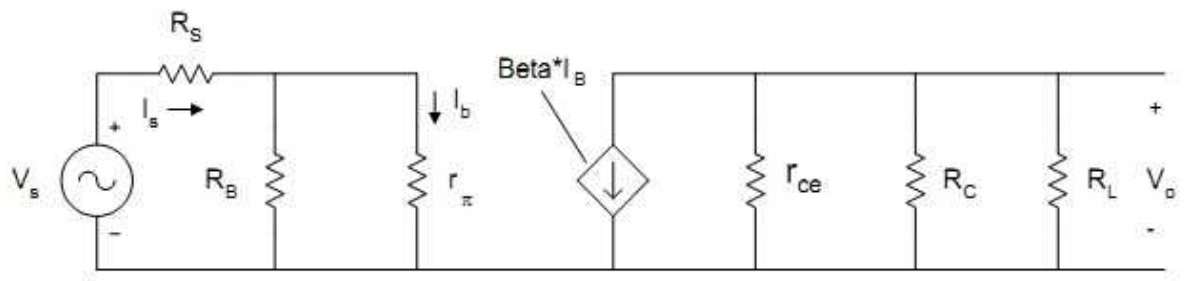

Figure 10: Equivalent circuit for calculating midband gain

From Figure 10, the midband gain, A_M , is

$$A_m = \frac{V_0}{V_S} = -\beta \left[r_{CE} \,\square\, R_C \,\square\, R_L \right] \left[\frac{R_B}{R_B + r_\pi} \right] \left[\frac{1}{R_S + \left[R_B \,\square\, r_\pi \right]} \right] \tag{24}$$

It can be shown that the low frequency poles, $\omega_{L1}, \omega_{L2}, \omega_{L3}$ can be obtained by the following equations

$$\tau_1 = \frac{1}{\omega_{L1}} = C_{C1} R_{IN} \tag{25}$$

$$\tau_2 = \frac{1}{\omega_{L2}} = C_{C1}\left[R_L + \left(R_C \,\square\, r_{ce}\right)\right] \tag{26}$$

$$\tau_3 = \frac{1}{\omega_{L3}} = C_E \left\{ R_E \,\square \left[\frac{r_\pi}{\beta_F + 1} + \left(\frac{R_B \,\square\, R_S}{\beta_F + 1} \right) \right] \right\} = C_E R_E^{'} \tag{27}$$

The high frequency equivalent circuit of the common-emitter amplifier is shown in Figure 11

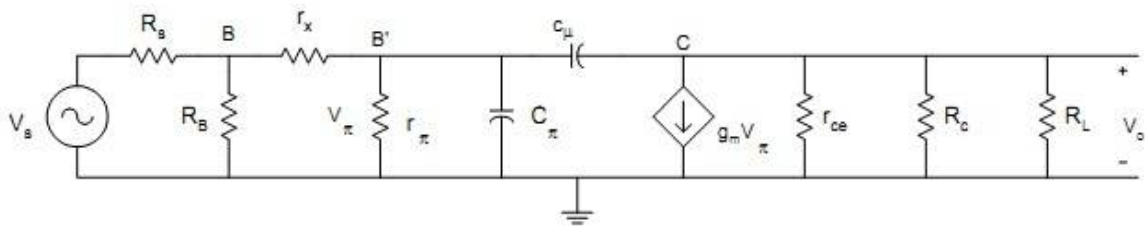

Figure 11: Equivalent circuit of CE amplifier at high frequencies

In Figure 11, C_μ is the collector-base capacitance, C_π is the emitter to base capacitance, r_X is the resistance of silicon material of the base region between the base terminal B and an internal or intrinsic base terminal B′. Using the Miller Theorem, it can be shown that the 3-dB frequency at high frequencies is approximately given as

$$\omega_H^{-1} = \left(r_\pi \,\square\left[r_x + \left(R_B \,\square\, R_S\right)\right]\right) C_T \tag{28}$$

where $C_T = C_\pi + C_\mu\left[1 + g_m\left(R_L \,\square\, R_C\right)\right]$ and $g_m = \frac{I_C}{V_T}$ w

In the following example, CEMTool is used to obtain the frequency response of a common-emitter amplifier.

Example 5

For a CE amplifier shown in Figure 9.

$\beta = 150, R_L = 1K\Omega, R_C = 4K\Omega, C_\pi = 100pF, V_{CC} = 10V, r_{CE} = r_O = 60K\Omega, C_{C1} = 2\mu F, C_{C2} = 4\mu F$

$C_E = 150\mu F, R_{B1} = 60K\Omega, R_{B2} = 40K\Omega, R_S = 100\Omega, r_x = 10\Omega$

Use CEMTool to plot the magnitude response of the amplifier.

Solution

Using Equations 25, 26, 27 and 28 are used to calculate the poles of Equation 23. The zero of the overall amplifier gain is calculated using Equation 24. The CEMTool program is as follows:

```
%Frequency response of CE Amplifier
rc=4e3; rb1=60e3; rb2=40e3; rs=100; rce=60e3;
re=1.5e3; rl=2e3; beta=150; vcc=10; vt=26e-3; vbe =0.7;
cc1=2e-6; cc2=4e-6; ce=150e-6;, rx=10; cpi=100e-12;
cmu=5e-12;
%   Ic is calculated
rb = (rb1 * rb2)/(rb1 + rb2);
vbb = vcc * rb2/(rb1 + rb2);
icq = beta * (vbb - vbe)/(rb + (beta + 1)*re);

% Calculation of low frequency poles
% using equations (12.67), (12.69) and (12.70)
rpi=beta * vt/icq;
rb_rpi=rpi * rb/(rpi + rb);
rin=rs + rb_rpi;
wl1=1/(rin * cc1);
rc_rce=rc * rce/(rc + rce);


wl2=1/(cc2 * (rl + rc_rce));
rb_rs=rb * rs/(rb + rs);
rx1=(rpi + rb_rs)/(beta + 1);
re_prime=re * rx1/(re + rx1);
wl3=1/(re_prime * ce);

% Calculate the low frequency zero using equation (12.72)
```

```
wz = 1/(re*ce);
% Calculate the high frequency pole using equation (12.74)
gm = icq/vt;
rbrs_prx = ( rb * rs/(rb + rs)) + rx;
rt = (rpi * rbrs_prx)/(rpi + rbrs_prx);
rl_rc = rl * rc/(rl + rc);
ct = cpi + cmu * (1 + gm * rl_rc);
wh = 1/(ct * rt);
% Midband gain is calculated
rcercrl = rce * rl_rc/(rce + rl_rc);
am = -beta * rcercrl * (rb/(rb + rpi)) * (1/(rin));



% Frequency response calculation using equation (12.65)
a4 = 1; a3 = wl1 + wl2 + wl3 + wh;
a2 = wl1*wl2 + wl1*wl3 + wl2*wl3 + wl1*wh + wl2*wh + wl3*wh;
a1 = wl1*wl2*wl3 +wl1*wl2*wh + wl1*wl3*wh + wl2*wl3*wh;
a0 = wl1*wl2*wl3*wh;
den=[a4 a3 a2 a1 a0];
b3 = am*wh;
b2 = b3*wz; b1 =0; b0 = 0;
num = [b3 b2 b1 b0];
w = logspace(1,10);
h = freqs(num,den,w);
mag = 20*log10(abs(h));
f = w/(2*pi);
% Plot the frequency response
plot(log10(f),mag)
title("Magnitude Response, 10^x")
xlabel("Frequency, Hz")
ylabel("Gain, dB")
axis([0, 10, 0, 45])
```

The frequency response is shown in Figure 12.

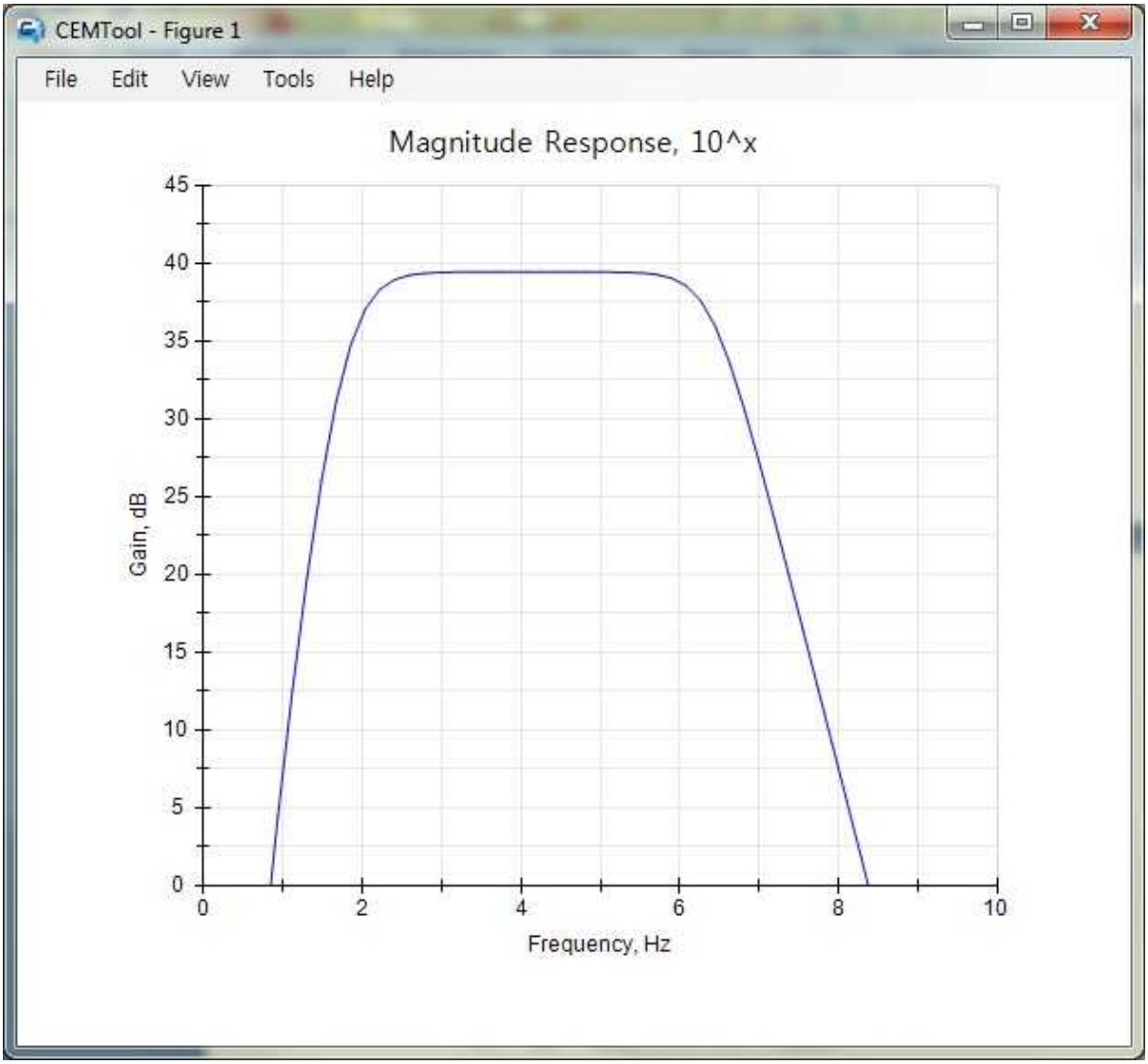

Figure 12: Frequency response of a CE amplifier

5. MOSFET characteristics

Metal-oxide-semiconductor field effect transistor (MOSFET) is a four-terminal device. The terminals of the device are the gate, source, drain, and substrate. There are two types of mosfets: the enhancement type and the depletion type. In the enhancement type MOSFET, the channel between the source and drain has to be induced by applying a voltage on the gate. In the depletion type mosfet, the structure of the device is such that there exists a channel between the source and drain. Because of the oxide insulation between the gate and the channel, mosfets have high input resistance. The electronic symbol of a mosfet is shown in Figure 13.

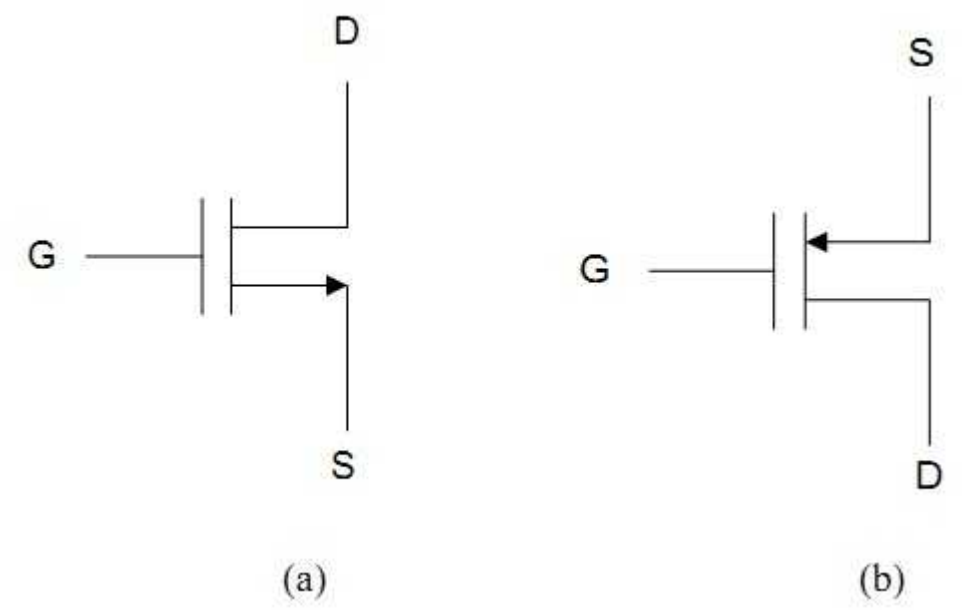

Figure 13: Circuit symbol of (a) N-channel and (b) P-channel MOSFETs

Mosfets can be operated in three modes: cut-off, triode, and saturation regions. Because the enhancement mode mosfet is widely used, the presentation in this section will be done using an enhancement-type mosfet. In the latter device, the channel between the drain and source has to be induced by applying a voltage between the gate and source. The voltage needed to create the channel is called the threshold voltage, V_T. For an n-channel enhancement-type mosfet, V_T is positive and for a p-channel device it is negative.

Cut-off Region

For an n-channel mosfet, if the gate-source voltage V_{GS} satisfies the condition $V_{GS} < V_T$ then the device is cut-off. This implies that the drain current is zero for all values of the drain-to-source voltage.

Triode Region

When $V_{GS} < V_T$ and V_{DS} is small, the mosfet will be in the triode region. In the latter region, the device behaves as a non-linear voltage-controlled resistance. The I-V characteristics are given by

$$I_D = k_n \left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2 \right] \tag{29}$$

Saturation Region

Mosfets can operate in the saturation region. A mosfet will be in saturation provided $V_{DS} > V_{GS} - V_T$ and I-V characteristics are given as

$$I_D = k_n \left(V_{GS} - V_T\right)^2 \tag{30}$$

In the following example, I-V characteristics and the locus that separates triode and saturation regions are obtained using CEMTool.

Example 6

For an n-channel enhancement-type MOSFET with k^n=1 mA/V^2 and V=1.5V, use CEMTool to sketch the I-V characteristics for V_{GS} = 4,6,8V and for V_{DS} between 0 and 12V .

Solution

CEMTool script

```
% I-V characteristics of mosfet
%
kn=1e-3; vt=1.5;
vds=0:12:0.5;
vgs=4:8:2;
m=length(vds);
n=length(vgs);

for (i=1;i<=n;i++)
{
    for (j=1;j<=m;j++)
    {
        if (vgs(i) < vt)
            cur(i,j)=0;
        else if (vds(j) >= (vgs(i) - vt))
            cur(i,j)=kn * (vgs(i) - vt)^2;
        else if (vds(j) < (vgs(i) - vt))
            cur(i,j)= kn*(2*(vgs(i)-vt)*vds(j) - vds(j)^2);

    }
}
plot(vds,cur(1,:),vds,cur(2,:),vds,cur(3,:))
xlabel("Vds, V")
ylabel("Drain Current,A")
title("I-V Characteristics of a MOSFET")
legend("Vgs = 4 V","Vgs = 6 V","Vgs = 8 V")
```

Figure 14 shows the I-V characteristics.

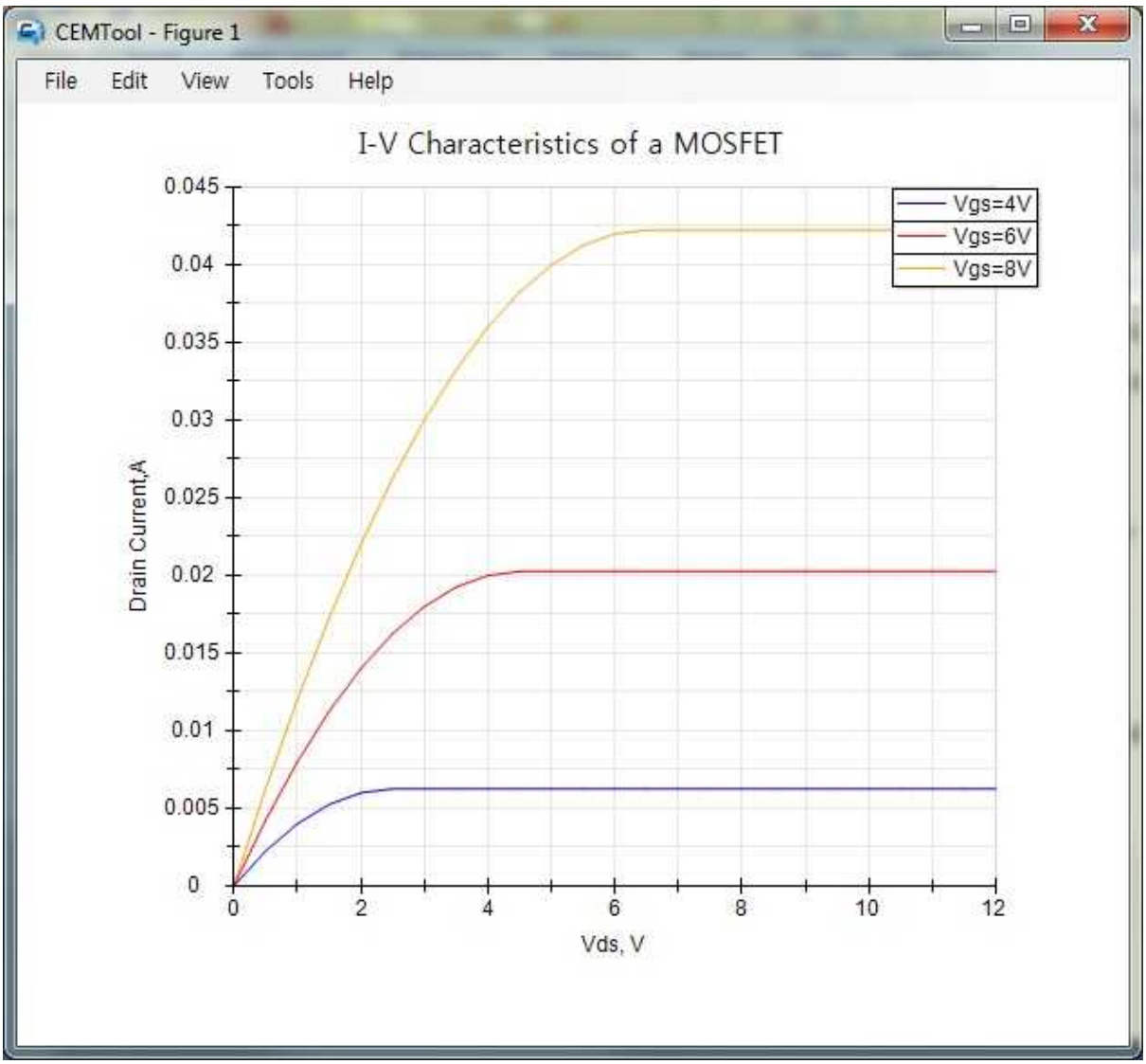

Figure 14: I-V characteristics of N-channel enhancement-type mosfet

6. Biasing of MOSFET circuits

A popular circuit for biasing discrete mosfet amplifiers is shown in Figure 15. The resistances R_{G1} and R_{G2} will define the gate voltage. The resistance R_S improves operating point stability. Because of the insulated gate, the current that passes through the gate of the MOSFET is negligible. The gate voltage is given as

$$V_G = \frac{R_{G1}}{R_{G1} + R_{G2}} V_{DD} \tag{31}$$

The gate-source voltage V_{GS} is $V_{GS} = V_G - I_S R_S$ (32)

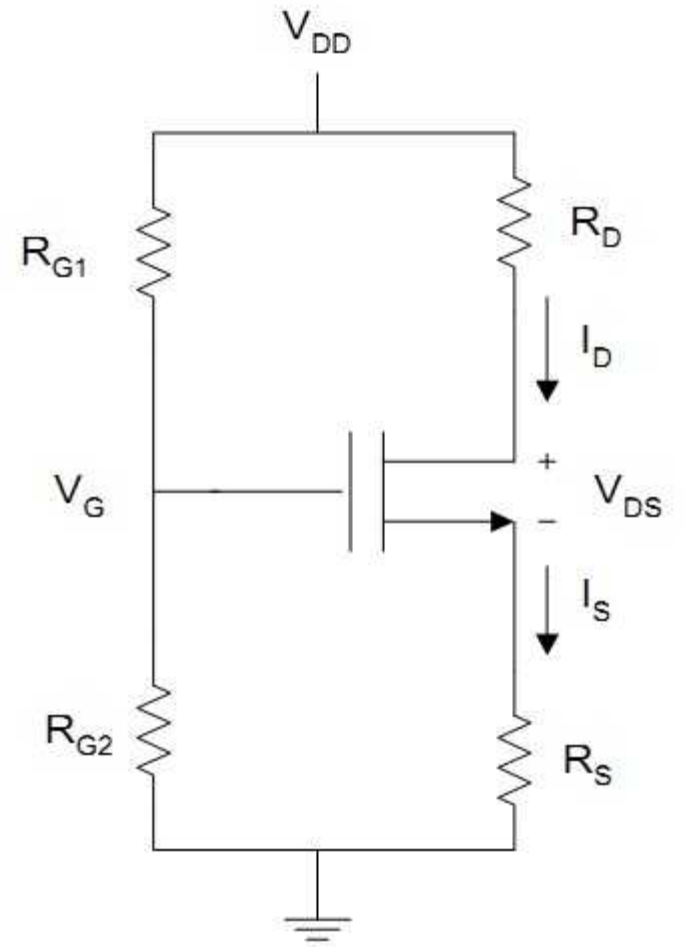

Figure 15: Simple biasing circuit for enhancement-type NMOS

For conduction of the MOSFET, the gate-source voltage V_{GS} should be greater than the threshold voltage of the mosfet, V_T. Since I_D=I_S, Equation 32 becomes

$$V_{GS} = V_G - I_D R_S \quad (33)$$

The drain-source voltage is obtained by using KVL for the drain-source circuit

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S = V_{DD} - I_D \left(R_D - R_S \right) \quad (34)$$

For proper operation of the bias circuits, $V_{GS} > V_T$ (35)

When Equation 35 is satisfied, the MOSFET can either operate in the triode or saturation region. To obtain the drain current, it is initially assumed that the device is in saturation and Equation 30 is used to calculate I_D. If Equation 30 is not satisfied, then Equation 29 is used to calculate I_D.

The method is illustrated by the following example.

Example 7:

For the circuit shown in Figure 16, $R_1 = 1.5M\Omega, L_1 = L_2 = 6\mu m, W_1 = 12\mu m, W_2 = 18\mu m$, $V_T = 2.0V$ and $V_{DD} = 5V$. Find the output current I_{D1}, V_{GS1}, I_0 and R_2. Assume that $V_0 = 2.5V, \mu C_{OX} = 30\mu A/V^2$. Neglect channel length modulation.

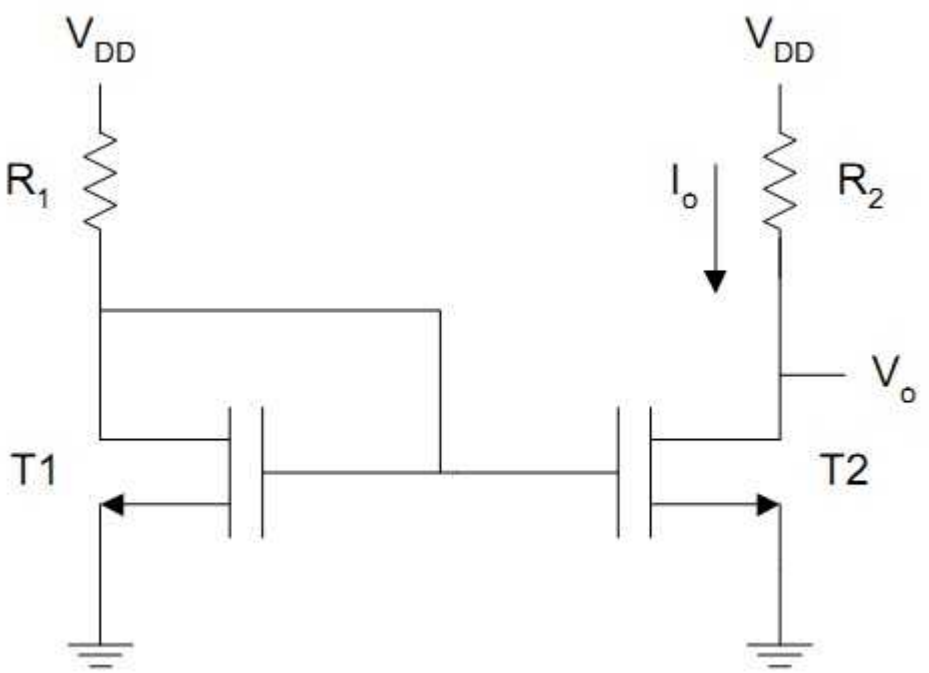

Figure 16: Circuit for example 7

Solution

Since T1 is in saturation, $I_{D1} = k_{n1}(V_{GS} - V_T)^2 = k_{n1}(V_{DS} - V_T)^2$

$V_{DS} = V_{DD} - I_{D1}R_1$

Thus, we obtain

$$I_0 = I_{D1}\left(\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right) \quad \text{and} \quad R = \frac{5 - V_0}{I_0}$$

The CEMTool script is as follows:

```
%
% Current mirror
%
ucox = 30e-6; l1 = 6e-6; l2 = 6e-6;
w1 = 12e-6; w2=18e-6;
r1=1.5e6; vt=2.0; vdd=5; vout=2.5;
```

```
% roots of quadratic equation(12.103) is obtained
kn = ucox * w1/(2 * l1);
a1 = r1^2;
a2 = -2*(vdd - vt)*r1 - (1/kn);
a3 = (vdd - vt)^2;
p = [a1,a2,a3];
i = roots(p);

% check for realistic value of drain current
vgs=vdd - r1*i(1);
if (vgs > vt)
   id1 = i(1);
   else
   id1 = i(2);


% output current is calculated from equation(12.100)
% r2 is obtained using equation (12.105)
iout = id1*w2*l1/(w1 * l2);
r2=(vdd - vout)/iout;

% print results
fprintf("Gate-source Voltage of T1 is")
vgs
fprintf("Drain Current of T1 is ")
 id1
fprintf("Drain Current Io is")
 iout
fprintf("Resistance R2 is")
 r2
```

The results are

```
Gate-source Voltage of T1 is
vgs =
      1.7305
Drain Current of T1 is
id1 =
```

1.8351e-006

Drain Current Io is

iout =

2.7527e-006

Resistance R2 is

r2 =

9.0821e+005

7. Frequency response of common-source amplifier

The common-source amplifier has characteristics similar to those of the common-emitter amplifier discussed in Section 12.4. However, the common-source amplifier has higher input resistance than that of the common-emitter amplifier. The circuit for the common source amplifier is shown in Figure 17

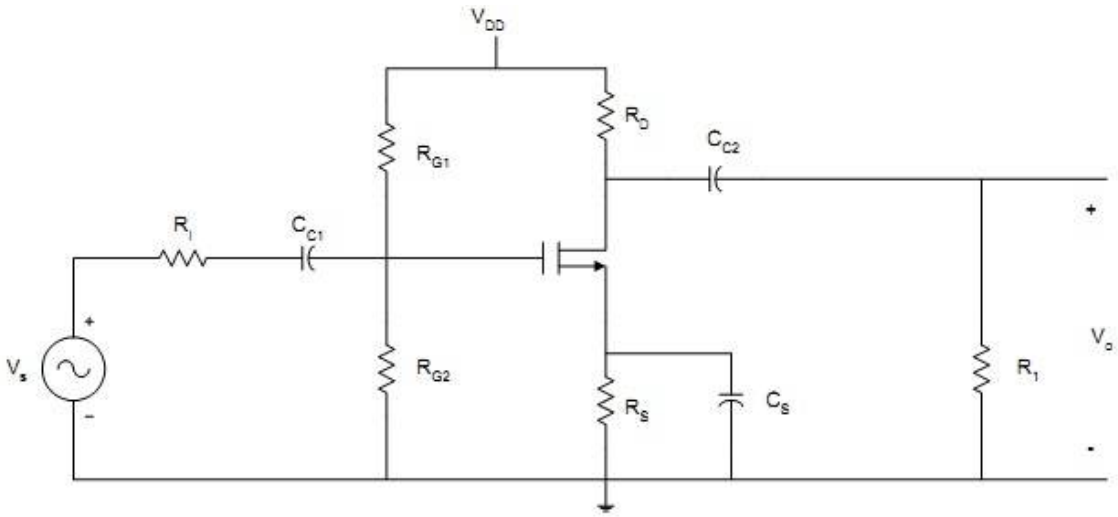

Figure 17: Common-Source amplifier

The external capacitors C_1, C_2, and C_S will influence the low frequency response. The internal capacitances of the FET will affect the high frequency response of the amplifier.

The midband gain, Am, is obtained from the midband equivalent circuit of the common-source amplifier. This is shown in Figure 18. The equivalent circuit is obtained by short-circuiting all the external capacitors and open-circuiting all the internal capacitances of the FET.

We can obtain the midband gain as $A_m = \frac{v_0}{v_s} = -g_m \left(\frac{R_G}{R_G + R_1} \right) (r_{ds} \square R_D \square R_L)$

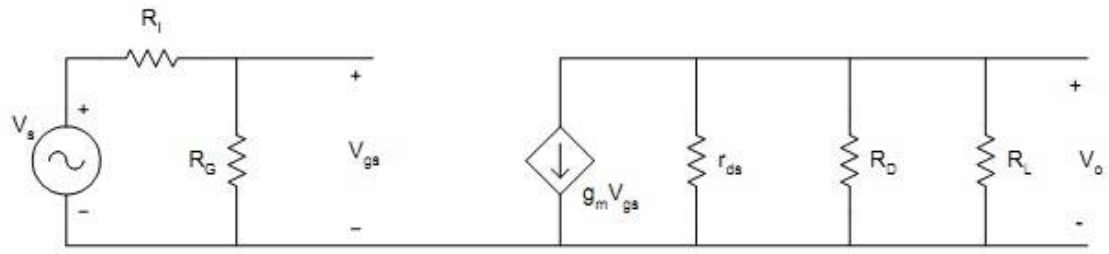

Figure 18: Midband equivalent circuit of common-source amplifier

In the following example, CEMTool is used to obtain the midband gain, cut-off frequencies and bandwidth of a common-source amplifier.

Example 8:

For the common-source amplifier, shown in Figure 17

$C_{C1} = C_{C2} = 1\mu F, C_s = 50\mu F,$ The FET parameters are

$C_{gd} = C_{ds} = 1pF, C_{gs} = 10pF, g_m = 10mA/V, r_{ds} = 50K\Omega$

$R_D = 8K\Omega, R_L = 10K\Omega, R_S = 2K\Omega, R_1 = 50\Omega, R_{G1} = 5M\Omega, R_{G2} = 5M\Omega$

Determine (a) midband gain, (b) the low frequency cut-off, (c) high frequency cut-off, and (d) bandwidth of the amplifier.

Solution

CEMTool script

```
%
% common-source amplifier
%
rg1=5e6; rg2=5e6; rd=8e3; rl=10e3;
ri=50; rs=2e3; rds=50e3;
cc1=1e-6; cc2=1e-6; cs=50e-6;
gm=10e-3; cgs=10e-12; cgd=1e-12; cds=1e-12;

% Calculate midband gain using equation (12.108)
a = (1/rds) + (1/rd) + (1/rl);
rlprime = 1/a;
rg = rg1*rg2/(rg1 + rg2);
gain_mb = -gm*rg*rlprime/(ri + rg);

% Calculate Low cut-off frequency using equation (12.113)
```

```
t1 = cc1*(rg + ri);
wl1 = 1/t1;
rd_rds = (rd*rds)/(rd + rds);
t2 = cc2 * (rl + rd_rds);
wl2=1/t2;
t3=cs * rs/(1 + gm * rs);
wl3=1/t3;
wl=sqrt(wl1^2 + wl2^2 + wl3^2);

% Calculate high frequency cut-off using equations (12.115 to12.119)
c1=cgs + cgd * (1 + gm * rlprime);
c2=cds + cgd;
rg_ri=rg * ri/(rg + ri);
wh1=1/(rg_ri * c1);
wh2=1/(rlprime * c2);
int_term = sqrt((1/wh1)^2 + (1/wh2)^2);
wh = 1/int_term;
bw = wh-wl;

%   Print results
fprintf("Midband Gain is ")
 gain_mb
fprintf("Low frequency cut-off is")
 wl
fprintf("High frequency cut-off is")
 wh
fprintf("Bandwidth is")
 bw
```

The results are

```
Midband Gain is
gain_mb =
   -40.8155
Low frequency cut-off is
wl =
   218.1808
High frequency cut-off is
wh =
```

```
    1.1676e+008
Bandwidth is
bw =
    1.1676e+008
```

References

1. CEMTool 6.0 User's Guide
2. John O. Attia, "Electronics and Circuit analysis using MATLAB", CRC Press, first edition 1999.